IN THE SPECIFICATION

Please amend the specification as shown below.

At page 7, please replace the paragraph beginning on line 35 with the following re-written paragraph:

--The pad area 21 includes a substrate 22. Substrate 22 has a first layer of metal 26, which is disposed above it. Metal layer 26 comprises a bottom metal (M1) layer, in one embodiment. Substrate 22 also has a second layer of metal 23, which is disposed above the first layer of metal 26. The ESDP device 25 is disposed below the first layer of metal 26. In one embodiment, the semiconductor structure 20 also has a layer of dielectric 24, which is disposed between second metal layer 23 and first metal layer 26. In one embodiment, a via 27 is disposed within the dielectric layer 24. Via 27 electrically couples the second metal layer 23 and first metal layer 26. In one embodiment, a via 27 connects to the ESDP device 25. Subsequent layers of metal can also be disposed between the first metal layer 26 and the second metal layer 23.--

At page 8, please replace the paragraph beginning on line 35 with the following re-written paragraph:

--Below second metal layer 424, a third metal layer 425 is disposed. A fourth metal layer 426 is disposed below third metal layer 425. An interlayer dielectric (ILD) 24 is disposed between third metal layer 425 and fourth metal layer 426. Third metal layer 425 and fourth metal layer 426 are electrically interconnected by via 27, which in one embodiment comprises a plurality of individual vias. A via 27 can electrically couple third layer of metal 425 and second layer of metal 424.--

At page 9, please replace the paragraph beginning on line 35 with the following re-written paragraph:

-- Below second metal layer 424, a third metal layer 425 is disposed. A fourth metal layer 426 is disposed below third metal layer 425. An interlayer dielectric (ILD) 24 is disposed between third metal layer 425 and fourth metal layer 426. Third metal layer 425 and fourth metal layer 426 are electrically interconnected by via 27, which in one embodiment comprises a plurality of individual vias. A via 27 can electrically couple third layer of metal 425 and second layer of metal 424.--

At page 11, please replace the paragraph beginning on line 40 with the following re-written paragraph:

-- ESDP transistor 711 comprises a source region 701 and a drain region 702, disposed within appropriately doped areas of substrate 22. ESDP transistor 711 also comprises a gate 703, which can be of a polycrystalline silicon II (POLY-II) or another gate material disposed above and between source region 701 and drain region 702, and beneath bottom metal layer 726. ESDP transistor 712 comprises a source region 704 and a drain region 705, disposed within appropriately doped areas of substrate 722. ESDP transistor 712 also comprises a gate 706, which can be of a POLY-II or another gate material disposed above and between source region 704 and drain region 705, and beneath bottom metal layer 726.--